

## REMARKS

Claims 1-16 are pending. The Examiner indicates allowability of claim 4 if rewritten in independent form including all of the limitations of the base and any intervening claims. The Examiner rejects claims 1-3 and 5-16 under 35 U.S.C. § 102(e) as being anticipated by Noji (U.S. Patent No. 6,138,255).

Applicants amend claims 1, 3, and 10, cancel claims 2, 4, and 13, and add claims 17 and 18. Claims 1, 3, 5-18 remain in the application.

Applicants add no new matter and request reconsideration.

### Claims Allowed

Applicants thank Examiner Nguyen for his indication of allowability of claim 4. Applicants amend claim 3 to incorporate the limitations of claim 4. Applicants cancel claim 4 without prejudice. Claims 3 and 5-9 are in condition for allowance.

### Claims Rejected Under § 102(e)

The Examiner alleges Noji teaches all of the elements recited in independent claims 1 and 10. Applicants disagree particularly as they amend claims 1 and 10.

Claim 1 recites *where during the test mode, the first plurality of external signals have a voltage level higher than a power supply voltage*. The Examiner points to Noji's signal 10S as disclosing the recited *first plurality of external signals*. Applicants point out that what is recited is a *plurality*, that is, two or more external signals, and not a single signal 10S as in Noji.

The Examiner alleges Noji discloses that "the level detecting circuit 60 detects whether the reference signals 10S has low, high, or same as external signal." Applicants believe this is error. Noji's signal 10S varies within the confines of the power supply voltage, e.g., VCC. It does not disclose applying a voltage *higher* than a power supply voltage at any time, much less specifically during the test mode. Noji describes its system as follows: "In the normal operation mode, the voltage level of the reference signal 10S is set at an intermediate level (e.g.,  $\frac{1}{2}$  a power voltage VCC) between a 'LOW' level and a 'HIGH' level of the input signals ADR[0]-ADR[n]. In a test mode, the voltage level of the reference signals 10S is set at the same 'BELOW' level as that of the input signals." Noji, column 4, lines 22-28.

Noji does not explain what exactly is meant by the term BELOW but one can surmise that if the term "intermediate" is described as  $\frac{1}{2}$  the power voltage VCC, then the term "BELOW" is likely less than  $\frac{1}{2}$  the power voltage. That is, during the test mode, the signal 10S is less than  $\frac{1}{2}$  the power voltage and not at a voltage level *higher* than the power supply level as recited. This interpretation is buttressed by an analysis of Noji's Figure 6. Claims 1 and 10-18 are therefore allowable.

Claim 17 recites "where the voltage level higher than the power supply voltage is applied only for a short period of time." A similar limitation rendered claim 4 allowable. This additional limitation should, therefore, also results in claim 17 being allowable.


Claim 10 now incorporates the limitations of cancelled claim 13.

### Conclusion

For the foregoing reasons, Applicants request reconsideration and allowance of all claims as amended. Applicants encourage the Examiner telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

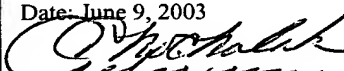
MARGER JOHNSON & McCOLLOM, P.C.

  
\_\_\_\_\_  
Scott A. Schaffer  
Reg. No. 38,610

MARGER JOHNSON & McCOLLOM  
1030 SW Morrison Street  
Portland, OR 97205  
(503) 222-3613

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date: June 9, 2003

  
\_\_\_\_\_  
Adrienne Chocholak